about 1-2 hours. Alternatively, for n-type doping, the drive in step may be performed at a temperature of up to about 1200° C. for up to about 24 hours.

An optional oxidation step, usually performed in a steam or oxygen ambient, can also be performed with or subsequent to the drive-in step, which forms a silicon dioxide layer (not shown) on the sidewalls and the bottoms of the trenches **422**. A thin layer of silicon nitride (not shown) can also be deposited on the sidewalls and the bottoms of the trenches **422**. Deposition of silicon nitride on thermally oxidized silicon wafers does not influence the fundamental properties of the Si—SiO_2 interface. The existence of silicon nitride makes surface potential stable or unstable according to the structures, partly due to the existence of hydrogen in silicon nitride. Hydrogen can influence electric properties. The layer of silicon nitride also serves the function to isolate and protect the silicon and silicon oxide from a refill material to be deposited in trenches **422**.

The lining of the trenches **422** with silicon nitride can be performed in general by CVD (thermal or plasma). The lining of the trenches **422** with silicon dioxide can be performed in general by CVD (thermal, plasma, or spun-on-glass (SOG)). The lining of the trenches **422** with silicon dioxide and/or silicon nitride can preferably be performed using application of tetraethylorthosilicate (TEOS) because of the better conformity achieved by TEOS. Preferably, the silicon nitride is about 100 Å to about 10,000 Å thick (1 μm=10,000 Å).

Referring to FIG. **4**C, the trenches **422** are then filled with a temporary or permanent refill material **428** such as a semi-insulating material, an insulating material, or a combination thereof. The refill material **428** can be a polysilicon, a re-crystalized polysilicon, a single crystal silicon, or a semi-insulating polycrystalline silicon (SIPOS). The trenches **422** may be filled using a SOG technique, CVD, surface reflow, or other methods known in the art. For example, the trenches **422** can be refilled with SIPOS. The amount of oxygen content in the SIPOS is selectively chosen to be between 2% and 80% to improve the electrical characteristics in the die **420**. Increasing the amount of oxygen content is desirable for electrical characteristics, but varying the oxygen content also results in altered material properties. Higher oxygen content SIPOS will thermally expand and contract differently than the surrounding silicon which may lead to undesirable fracturing or cracking especially near the interface of differing materials. Accordingly, the oxygen content of the SIPOS is optimally selected to achieve the most desirable electrical characteristics without an undesirable impact on mechanical properties.

It will be appreciated by those skilled in the art that changes could be made to the embodiments described above without departing from the broad inventive concept thereof. It is understood, therefore, that the invention is not limited to the particular embodiments disclosed, but it is intended to cover modifications within the spirit and scope of the present invention as defined by the appended claims.

We claim:

1. A superjunction device comprising:

(a) a semiconductor wafer, the semiconductor wafer including at least one die;

(b) at least one first trench formed in the at least one die, the at least one first trench having a first orientation and defining a first area; and

(c) at least one second trench formed in the at least one die, the at least one second trench having a second orientation that is different from the first orientation, the at least one second trench defining a second area such that a ratio of the first area to the second area is about one-to-one.

2. The device of claim **1**, further comprising:

(d) at least one additional trench formed in the at least one die, the at least one additional trench having an orientation that is different from at least one of the first orientation and the second orientation.

3. A superjunction device comprising:

(a) a semiconductor wafer, the semiconductor wafer including at least one die;

(b) a first plurality of trenches in the at least one die, each of the first plurality of trenches having a first orientation, the first plurality of trenches defining a first area; and

(c) a second plurality of trenches in the at least one die, each of the second plurality of trenches having a second orientation that is different from the first orientation, the second plurality of trenches defining a second area such that a ratio of the first area to the second area is about one-to-one.

4. The device of claim **3**, wherein

(i) each of the first plurality of trenches has a length dimension, the length dimension of each of the first plurality of trenches being different from at least one other of the first plurality of trenches; and

(ii) each of the second plurality of trenches has a length dimension, the length dimension of each of the second plurality of trenches being different from at least one other of the second plurality of trenches.

5. The device of claim **3**, wherein

(i) each of the first plurality of trenches has a length dimension, the length dimension of each of the first plurality of trenches being identical; and

(ii) each of the second plurality of trenches has a length dimension, the length dimension of each of the second plurality of trenches being identical.

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